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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/825,027	04/02/2001	David Michael Rogers	AMD-E1019	6915

7590 03/17/2004

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EXAMINER	
KOBERT, RUSSELL MARC	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/825,027	ROGERS ET AL.	
	Examiner	Art Unit	
	Russell M Kobert	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-108* is/are pending in the application.

4a) Of the above claim(s) *30-108* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7-15,19 and 22-29* is/are rejected.

7)☒ Claim(s) *2-10,16-18,20,21 and 23-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. Applicant's election without traverse of Invention I, Species 1 and Sub-Species 1, claims 1-29, in the Election filed August 12, 2003 is acknowledged.

2. Claims 30-108 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Invention and/or Species, there being no allowable generic or linking claim. Election was made **without** traverse in the Election filed August 12, 2003.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings, with respect to the Species election (Figure 1), must show every feature of the invention specified in the claims. Therefore, the driver circuit and bias circuit described in claim 7, the digital to analog converter coupled to the first and second transistor pairs described in claim 16, the field continuation structures described in claims 20 and 21, the device under test comprising a field effect transistor described in claim 23, the device under test comprising a field effect transistor floating gate memory transistor and the device under test comprising one field effect transistor of a plurality of field effect transistors described in claim 29 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. Claims 7-10, 16-18, 20, 21 and 23-29 are objected to as having claimed subject matter excluded from the elected Species (Figure 1) noted supra.

5. Claims 22-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what Applicants regard as their invention. Is the invention drawn to a device for testing or a device under test? It appears Applicants are claiming a device for testing and as such, examination of the claimed subject matter will be limited to the apparatus for testing, not the device under test. Thus, any claimed limitations to the device under test are not considered to add patentable weight to the claimed device for testing.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 7-15, 19 and 22-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al (An On-Chip, Attofarad Interconnect Charge-Based Capacitance Measurement (CBCM) Technique, Chen, J.C.; McGaughy, B.W.; Sylvester, D.; Chenming Hu, Electron Devices Meeting, International, 8-11 Dec. 1996, Pages: 69 - 72).

Chen et al anticipates a test circuit (Figure 1) comprising:

a first transistor pair including a first transistor (upper-right transistor) and a second transistor (lower-right transistor) coupled with a device under test (Metal 1 and Metal 2 crossing; located to the right of the first transistor pair); and

a second transistor pair including a third transistor (upper-left transistor) and a fourth transistor (lower-left transistor) coupled with a dummy device (Metal 1; located to the left of the second transistor pair), the first transistor and the third transistor having a first common gate connection configured to be driven by a first variable voltage (V_2; see also Figure 2), the first transistor and the third transistor being biased by a first variable bias voltage (V_{DD}), the second transistor and the fourth transistor having a second common gate connection configured to be driven by a second variable voltage (V_1; see also Figure 2), the second transistor and the fourth transistor being biased by a second variable bias voltage (Ground); as recited in claim 1. Moreover, the limitations of claims 7-10 are considered inherent in the apparatus of Chen et al or are within the normal range of operating the apparatus of Chen et al.

As to claim 11, Chen et al further describes (see Figure 1, Signal Generator) the added limitation of a clock signal generating circuit coupled with

the first common gate connection and the second common gate connection and configured to generate the first variable voltage and the second variable voltage. Moreover, the limitations of claims 12-15 are considered inherent in the apparatus of Chen et al or are within the normal range of operating the apparatus of Chen et al.

As to claim 19, Chen et al further describes (see page 3.4.4, Section IV. Discussion, lines 6-10) the device under test and the dummy device comprising multiple electrode capacitances.

As to claim 22, Chen et al further shows (Figure 3) the device under test comprising an active semiconductor device. Claims 23-29 are anticipated by Chen et al because the added limitations are not considered to add patentable weight to the device for testing described in claim 22.

8. Claims 1, 7-15, 19 and 22-29 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by McGaughy et al (A Simple Method for On-Chip, Sub-Femto Farad Interconnect Capacitance Measurement, McGaughy, B.W.; Chen, J.C.; Sylvester, D.; Chenming Hu; Electron Device Letters, IEEE ,Volume: 18, Issue: 1 , Jan. 1997, Pages: 21 – 23).

9. Claims 1, 7-15, 19 and 22-29 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Fan et al (6404222).

10. The following is a statement of reasons for the indication of allowable subject matter:

Claims 2-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The additional limitation of the first, second, third and fourth transistors comprising p-channel transistors; described in claim 2 has not been found. It is further noted that the examiner's reasons are understood to be predicated upon consideration of each of the claims as a whole, and not upon any specific elements of the claims.

11. A shortened statutory period for response to this action is set to expire three month(s) from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell Kobert whose telephone number is (571) 272-1963. The Examiner's Supervisor, Kammie Cuneo, can be reached at (571) 272-1957. For an automated menu of Tech Center 2800 phone numbers call (571) 272-2800.

Russell M. Kobert
Patent Examiner
Group Art Unit 2829
January 16, 2004

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